WHAT IS CLAIMED IS:

1. A PFC-PWM controller having a power saving means comprising:

an input voltage terminal;

a PFC-feedback voltage terminal;

a PWM-feedback voltage terminal;

a first reference voltage terminal;

a second reference voltage terminal;

an input resistor;

a detection pin connected to said input resistor;

a current synthesizer for providing a bias current, wherein said current synthesizer has at least four inputs, wherein a first input is connected to said PWM-feedback voltage terminal, a second input is connected to said first reference voltage terminal, a third input is connected to said PFC-feedback voltage terminal, and a fourth input is connected to said second reference voltage terminal;

an oscillator having an input for receiving said bias current, a first output for generating a pulse signal, and a second output for generating a first saw-tooth signal;

a pulse-width limiter having a first input for receiving said pulse signal, a second input for receiving said first saw-tooth signal, and an output for generating a limit signal;

a saw-wave generator for generating a second saw-tooth signal; and

a current reference generator having an input connected to the input voltage terminal via said input resistor and an output for generating a template signal.

2. The PFC-PWM controller as claimed in claim 1 further comprising:

an input RMS voltage terminal;

a current-sense terminal;

a NOT-gate for receiving the pulse signal;

a first SR flip-flop having a set-input connected to an output of said NOT-gate;

an AND-gate having a first input for receiving said limit signal, a second input for receiving an output of said first SR flip-flop, and an output for generating a PWM signal, wherein the maximum on-time of said PWM signal is determined by said limit signal;

a second SR flip-flop having a set-input for receiving said pulse signal;

a first comparator for PWM control having a positive input connected to the PWM-feedback voltage terminal, a negative input for receiving the first saw-tooth signal, and an output for resetting said first SR flip-flop; and

a multiplier/divider circuit having at least three inputs, wherein a first input is connected to said output of said current reference generator, a second input is connected to said input RMS voltage terminal, and a third input is connected to said PFC-feedback voltage terminal.

3. The PFC-PWM controller as claimed in claim 1 further comprising:

a buffer-gate for generating a PFC signal coupled to an output of a second SR flip-flop;

an error amplifier circuit for generating a feedback voltage having a first input connected to an output of the multiplier/divider circuit and a second input connected to a negative output of said bridge rectifier and an output;

a second comparator for PFC control having a negative input connected to an output of said saw-wave generator, a positive input for receiving said feedback voltage, and an output for setting said second SR flip-flop; and

a start-up diode for starting up the PFC-PWM controller.

4. The PFC-PWM controller as claimed in claim 1, wherein said current synthesizer comprises:

a first V-to-I transistor for producing a PWM-feedback current;

a first operational amplifier for driving said first V-to-I transistor, wherein a positive input of said first operational amplifier is connected to said PWM-feedback voltage terminal;

a first buffer amplifier having a positive input connected to said first reference voltage terminal; and

a first resistor, wherein said first resistor is connected between a negative input of said first operational amplifier and a negative input of said first buffer amplifier.

5. The PFC-PWM controller as claimed in claim 4, wherein said PWM-feedback current is generated by applying a first voltage across said first resistor, wherein the magnitude of said first voltage is equal to the magnitude of a first reference voltage subtracted from the magnitude of a PWM-feedback voltage.

6. The PFC-PWM controller as claimed in claim 4, wherein said current synthesizer further comprises:

a second V-to-I transistor for producing a PFC-feedback current;

a second operational amplifier for driving said second V-to-I transistor, wherein a positive input of said second operational amplifier is connected to said PFC-feedback voltage terminal;

a second buffer amplifier having a positive input connected to said second reference voltage terminal; and

a second resistor, wherein said second resistor is connected between a negative input of said second operational amplifier and a negative input of said second buffer

amplifier.

7. The PFC-PWM controller as claimed in claim 6, wherein said PFC-feedback current is generated by applying a second voltage across said second resistor, wherein the magnitude of said second voltage is equal to the magnitude of a second reference voltage subtracted from the magnitude of a PFC-feedback voltage.

8. The PFC-PWM controller as claimed in claim 4, wherein said current synthesizer further comprises:

a first current mirror for supplying a first mirror-current, wherein said first current mirror has a first input-transistor coupled with a first output-transistor;

a second current mirror for supplying a second mirror-current, wherein said second current mirror has a second input-transistor coupled with a second output-transistor; and

a limit current source for clamping said bias current, wherein the amplitude of said bias current is equal to the sum of said first mirror-current and said second mirror-current.

9. The PFC-PWM controller as claimed in claim 1, wherein said oscillator comprises:

a first saw-tooth capacitor for generating said first saw-tooth signal;

a charge current source for providing a charge current;

a third current mirror for mirroring a first discharge current, wherein said third current mirror has a third input-transistor coupled with a third output-transistor, wherein a drain of said third input-transistor receives said bias current and a drain of said third output-transistor draws said first discharge current from said first saw-tooth capacitor;

an upper-threshold comparator for initiating the pulse signal;

a lower-threshold comparator for terminating the pulse signal;

a first NAND-gate;

a second NAND-gate, wherein an output of said second NAND-gate is connected to an input of said first NAND-gate;

a first switch coupled to said first saw-tooth capacitor, wherein said first saw-tooth capacitor is charged by said charge current when said first switch is closed;

a second switch coupled to said first saw-tooth capacitor, wherein said first saw-tooth capacitor is discharged by said first discharge current when said second switch is closed, wherein said second switch is controlled by an output of said first NAND-gate; and

a NOT-gate for controlling said first switch, wherein said NOT-gate has an input connected to said output of said first NAND-gate.

10. The PFC-PWM controller as claimed in claim 1, wherein said pulse-width limiter comprises:

a third comparator for controlling a pulse-width of said limit signal, wherein said third comparator has a positive input for receiving said first saw-tooth signal and a negative input connected to a third reference voltage terminal, wherein the pulse-width of said limit signal is determined by the magnitude of a third reference voltage;

a third NAND-gate having a first input for receiving said pulse signal; and

a fourth NAND-gate having a first input connected to an output of said third NAND-gate, a second input connected to an output of said third comparator, and an output for supplying said limit signal.

11. The PFC-PWM controller as claimed in claim 1, wherein said saw-wave generator comprises:

a supply voltage terminal;

a second saw-tooth capacitor for generating said second saw-tooth signal;

a third switch having an input connected to a fourth reference voltage terminal, wherein said third switch has an output coupled to said second saw-tooth capacitor;

a first transistor having a gate driven by said pulse signal, wherein said first transistor has a source connected to the ground reference;

a discharge current source coupled between said supply voltage terminal and a drain of said first transistor; and

a fourth current mirror for mirroring a second discharge current, wherein said fourth current mirror has a fourth input-transistor coupled with a fourth output-transistor, wherein said fourth current mirror receives a current from said discharge current source, wherein said fourth current mirror discharges said second saw-tooth capacitor.

12. The PFC-PWM controller as claimed in claim 1, wherein said current reference generator comprises:

a fifth reference voltage terminal;

a second transistor having a gate connected to said fifth reference voltage terminal, wherein said second transistor has a drain connected to said input voltage terminal via said input resistor; and

a fifth current mirror having a fifth input-transistor coupling with a fifth output-transistor, wherein said fifth current mirror receives a current from a source of said second transistor, and wherein said fifth current mirror supplies said template signal.